REMARKS

The claims are claims 1, 2, 4, 5, 10, 11, 13 and 15 to 33.

Claims 4, 10, 20 and 23 are amended. Claim 12 is canceled. New claims 25 to 33 are added. Claim 4 has been amended to depend upon claim 1 rather than canceled claim 3. Claim 10 has been amended to distinguish over the rejection. Claim 20 has been amended to correct an error noted by the Examiner and to distinguish over the rejection. Claim 23 has been amended to change "said predetermined address boundary" to "a predetermined address boundary." New claim 25 corresponds generally to prior claim 10 except that it recites an operand field of the conditional branch-decrement instruction designates the test register as described in the application at page 22, line 27 to page 23, line 5 and illustrated at field 502 in Figure 5. New claim 26 corresponds to claim 20 except dependent upon claim 25. New claim 27 recites the branch address is a combination of a displacement field of the conditional branch-decrement instruction and the program counter contents as described in the application at page 23, lines 6 to 19 and illustrated at field 504 in Figure 5. New claim 28 recites the combination is addition of a signed displacement value. New claim 29 recites the combination is a shift and addition of a signed displacement value. New claim 30 corresponds to prior claim 10 except it recites the branch address is a combination of a displacement field of the conditional branch-decrement instruction and the program counter contents. New claims 31 to 33 correspond to respective claims 26, 28 and 29 except dependent upon claim 30.

Claims 4 and 20 were objected to for informalities. Claim 4 has been amended to depend upon claim 1 rather than canceled claim 3. Claim 20 has been amended to recite "steps" rather than "step."

The Applicants respectfully submit that these amendments cure the informalities.

Claim 23 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The FINAL REJECTION states that claim 23 recites the limitation "said predetermined address boundary" in line 5. Claim 23 has been amended to change "said predetermined address boundary" to "a predetermined address boundary." The Applicants respectfully submit that this amendment cures the indefiniteness.

Claims 10, 13 and 20 were rejected under 35 U.S.C. 102(b) as anticipated by the Intel *Pentium Processor Family Developer's Manual Vol. 3: Architecture and Programming Manual*. The FINAL REJECTION states the Intel publication teaches: (1) testing a test register selected by the conditional branch-decrement instruction to determine if the contents of the test register meet a first condition; and (2) providing a branch address to a program counter to cause a branch if the contents of the test register meet the first condition.

Amended claim 10 recites subject matter that is not anticipated by the Intel publication. Claim 10 recites the test register is "selected by the conditional branch-decrement instruction from among a plurality of distinct data registers." The Applicants respectfully submit that the CX and ECX registers taught in the Intel publication are not plural distinct data registers as recited in amended claim 10. The Intel publication teaches that the CX and ECX data registers are parts of a single data register and that the ECX data register includes all the contents of the CX data register. Therefore these are not plural distinct data registers as required by claim 10. Accordingly, claim 10 is not anticipated by the Intel publication.

Claim 10 recites further subject matter not anticipated by the Intel publication. Claim 10 recites "providing a branch address to a program counter to cause a branch." The Intel publication fails to teach such a branch. Instead, the Intel publication teaches that string operation of the instruction following the repeat prefix is repeated. This is not a branch as recited in claim 10. The FINAL REJECTION cites servicing a pending interrupt and the IF-THEN-ELSE constructs as the branch. The Applicants respectfully submit that any program branch in response to a pending interrupt is caused by the interrupt and not by the repeat string instruction. The IN-THEN-ELSE constructs on page 25-267 do not correspond to program counter branches. This construct is rather a logical description of the instruction operation in the same fashion as Table 8 on page 24 of this application. This same logical operation is described in the text steps 1 to 7 at lines 11 to 16 of page 25-268. Regardless of the manner of description, the Intel publication states that the string operation repeats upon satisfaction of the condition in the test register. Thus this in not the program branch recited in claim 10. Accordingly, claim 10 is not anticipated by the Intel publication.

Claim 20 recites subject matter not anticipated by the Intel publication. Claim 20 recites "a plurality of distinct general purpose registers" and "designating via the conditional branch-decrement instruction one of said general purpose registers as said selected test register." The Applicants respectfully submit that the CX and ECX data registers are not the plurality of distinct general purpose data registers from which the test register is designated. The Intel publication teaches that the CX and ECX data registers are parts of a single data register and that the ECX data register includes all the contents of the CX data register. Therefore these are not plural distinct data registers as required

by claim 20. Accordingly, claim 20 is not anticipated by the Intel publication.

Claims 11, 13 and 21 to 24 are allowable by dependence upon allowable claim 10.

New claims 25 to 33 recite subject matter not anticipated by the Intel publication. New claim 25 recites the test register is "selected by an operand field of the conditional branch-decrement instruction." The Intel publication teaches that the CX or ECX data register is selected dependent upon current address size. Claims 26 and 31 recite "a plurality of distinct general purpose registers" and "designating via the conditional branch-decrement instruction one of said general purpose registers as said selected test register." The Intel publication teaches that the CX and ECX data registers are parts of a single data register and that the ECX data register includes all the contents of the CX data register. Therefore these are not plural distinct data registers as required by claims 26 and 31. Claims 27 and 30 recite that the branch address is a combination of a displacement field of the conditional branch-decrement instruction and the program counter contents. The Intel publication does not teach a displacement field combined with the current program counter. Claims 28 and 32 recite the combination is addition of a signed displacement value. The Intel publication fails to teach addition of a signed displacement value. Claims 29 and 33 recite the combination is a shift and addition of a signed displacement value. The Intel publication does not teach this shift and signed addition combination.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment is in response to a completely new rejection first presented in the FINAL REJECTION.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early

entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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